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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/753,055	12/28/2000	David William Boerstler	AUS920000518US1	9311

7590 07/07/2004

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EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2634	8

DATE MAILED: 07/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/753,055	BOERSTLER, DAVID WILLIAM	
	Examiner	Art Unit	
	YOUNG T. TSE	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-17* is/are rejected.

7)☒ Claim(s) *9 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3,6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: on page 1, line 4, "Serial No. __ / _____" should be changed to – Serial No. 09/753,055 – and lines 5-6, the phrase "(attorney docket number AUS9-2000-0518)" should be deleted; on page 10, line 26, "Serial No. __ / _____" should be changed to – Serial No. 09/726,282 – and line 28, "which is" should be changed to – now U. S. Patent No. 6,559,729 B2, which is --. Appropriate correction is required. For the formality of the application under the present office practice, applicant(s) is required to replace "Claims" with "I or We Claim", "The Invention Claimed Is" (or the equivalent) before the Claims part of the specification of the instant application. See MPEP 608.01(m).

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. Claims 1-18 are objected to because of the following informalities: in claim 1, lines 4 and 8-9, "the multiphase signals" should be changed to – the multiphase clock signals --; in claim 2, line 2, "multiphase clock signals" should be changed to – the multiphase clock signals --; in claim 10, lines 5 and 10, "the

multiphase signals" should be changed to – the multiphase clock signals --; in claim 11, line 2, "multiphase clock signals" should be changed to – the multiphase clock signals --; wherein claims 3-9 and 12-18 are depended directly or indirectly upon claims 1 and 10. Appropriate correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8 and 10-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen.

Chen (U.S. Patent No. 5,850,422) discloses a clock/data recovery circuit 10 in Figure 1 includes an analog PLL (phase locked loop) 12, an input data 36, and a digital PLL 13. The digital PLL 13 includes a data sampler 14, a clock multiplexer 16, a lead/lag phase detector 18, a loop filter 20, and a pulse swallower 22 (col. 3, lines 52-58).

Figure 2 discloses the detailed embodiment of the analog PLL 12 of Figure 1.

Figure 3 discloses the detailed embodiment of the data sampler 14 of Figure 1.

Figure 4 discloses the detailed embodiment of the clock multiplexer 16 of Figure 1.

Figure 5 discloses the detailed embodiment of the pulse swallower 22 of Figure 1.

Figure 6A discloses the detailed embodiment of the lead/lag phase detector 18 of Figure 1.

Figure 7 discloses the detailed embodiment of the loop filter 20 of Figure 1.

With respect to claims 1 and 10, the analog PLL 12 provides ten pultiphase clock signals P0-P9; the clock multiplexer 16 selects one of the multiphase clock signals based on a plurality of synchronization states OP0-OP9 generated by the data sampler 14 identifying which of the multiphase clock signals is most closely aligned with the data stream 40; and the lead/lag phase detector 18 samples the data stream 40 using the selected one of the multiphase clock signals to produce a recovered clock and a retimed data.

With respect to claims 2 and 11, it is well known in the art that the multiphase clock signals are subharmonics of the data stream 40.

With respect to claims 3, 5, 12, and 14, the multiphase clock signals are either early or late with respect to the data stream 40 because the phase detector 18 is a lead/lag phase detector. Also see the table of Figure 6B.

With respect to claims 4 and 13, D-type flip-flops 50 are used in the lead/lag phase detector 18 (Figure 6A).

With respect to claims 6-7 and 15-16, the clock phases P0-P9 are generated by a 5-stage VCO 30 and the phase errors generated by a phase/frequency detector 24 are inputted to a charge pump 26 of the analog PLL 12 (Figure 2).

With respect to claims 9 and 17, although the retimed data output by the lead/lag phase detector 18 is shown as one retimed data, bud based on one selected multiphase clock signals only. In other words, if the selector selects other clock signals or more than one clock signals, the lead/lag phase detector 18 will generate a plurality of retimed data.

Allowable Subject Matter

5. Claims 9 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to show or suggest that the a PLL combines respective pairs of retime state signals and inverted phase signals using a plurality of respective AND gates and uses the output of the OR gates to produce the retimed data signal.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

References Nelson, Brown, Chai et al., Dreps et al., Huang, and Duffy et al. are related to phase locked loop circuits comprising a multiphase oscillator circuit for generating a plurality of multiphase clock signals, a clock selector for selecting one of the multiphase clock signals, and a multiphase phase detector

for detecting a data stream and the selected clock signal to generate a retimed data signal and a recovery clock signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Young Tse** whose telephone number is **(703) 305-4736**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Stephen Chin**, can be reached at **(703) 305-4714**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

P.O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal
Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Young T. Tse
Primary Examiner
6/27/04